Polysilicon characterization by XRD/TEM /RAMAN techniques

Giuseppe Moccia – Lfoundry

Vanda Granato – Lfoundry

Luca Lozzi - University of L'Aquila

Maurizio Passacantando -University of L'Aquila

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INTRODUCTION

•*Polysilicon properties strongly depend on the deposition process and temperature.*

•*The deposited films go through an amorphous – crystalline transition phase around 580°C – 650°C temperature range. Hence, films deposited in the transition region of this temperature range can show drastic changes in the crystallinity and the morphology.*

•*To achieve desired properties of the transistor channel poly-Si, grain size, resistivity, mobility and interface quality must be carefully monitored and controlled.*

•*One of the important parameters of the transistor poly-Si channel is the grain size. Since it modulates the channel carrier mobility.*

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INTRODUCTION

•*The grain size measurement methods, X-ray diffraction (XRD) and transmission electron microscopy (TEM) are frequently used, but these techniques are time consuming, lacks spatial resolution or destructive.*

•*Micro-Raman spectroscopy (Raman), that is currently recognized as a powerful tool in identifying stress and strain in silicon, is another technique that can be applied in poly grain size characterization.*

•*As the method is contactless, no sample preparation is required. Other advantages of Raman measurements are: non-destructive, fast, with high spatial resolution and high sensitivity.*

In this work, XRD, TEM and Raman measurements were used to evaluate poly-Si grain size of polycrystalline silicon (poly-Si) growth in a vertical LPCVD reactor. This should be considered a first step of an overall characterization of transistor poly-Si gate including implant poly doping and annealing processes as well.

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SAMPLE

•The analyzed samples were prepared on Si(1 0 0) p-type substrates coated with 100 nm of SiO_2. The films were deposited in the LPCVD vertical furnace at temperature range of 620–634 C and at pressures of 100mT and SiH_4 at250sccm.

wf ID	Poly dep Temperature	Wafer Furnace position
T158079-12	620	Top
T145109-23	630	Top
T152769-20	634	Top

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XRD Analysis

- *The crystallographic orientations of the films were examined by x-ray diffraction*
- *The grain size of the polysilicon films was estimated by using the Sherrer formula :*

$$Mean\ particle\ size = \frac{0.9\,\lambda}{\beta \cos\theta}$$

λ= X-ray wavelength
β = line broadening at full width half maximum (FWHM) of the peak
θ = angle of the peak used for the analysis

Instrument: SIEMENS D5000
Tube: Cu anode, with Cu Kα1 (1.54056 Å) and Cu Kα2 (1.54439 Å)

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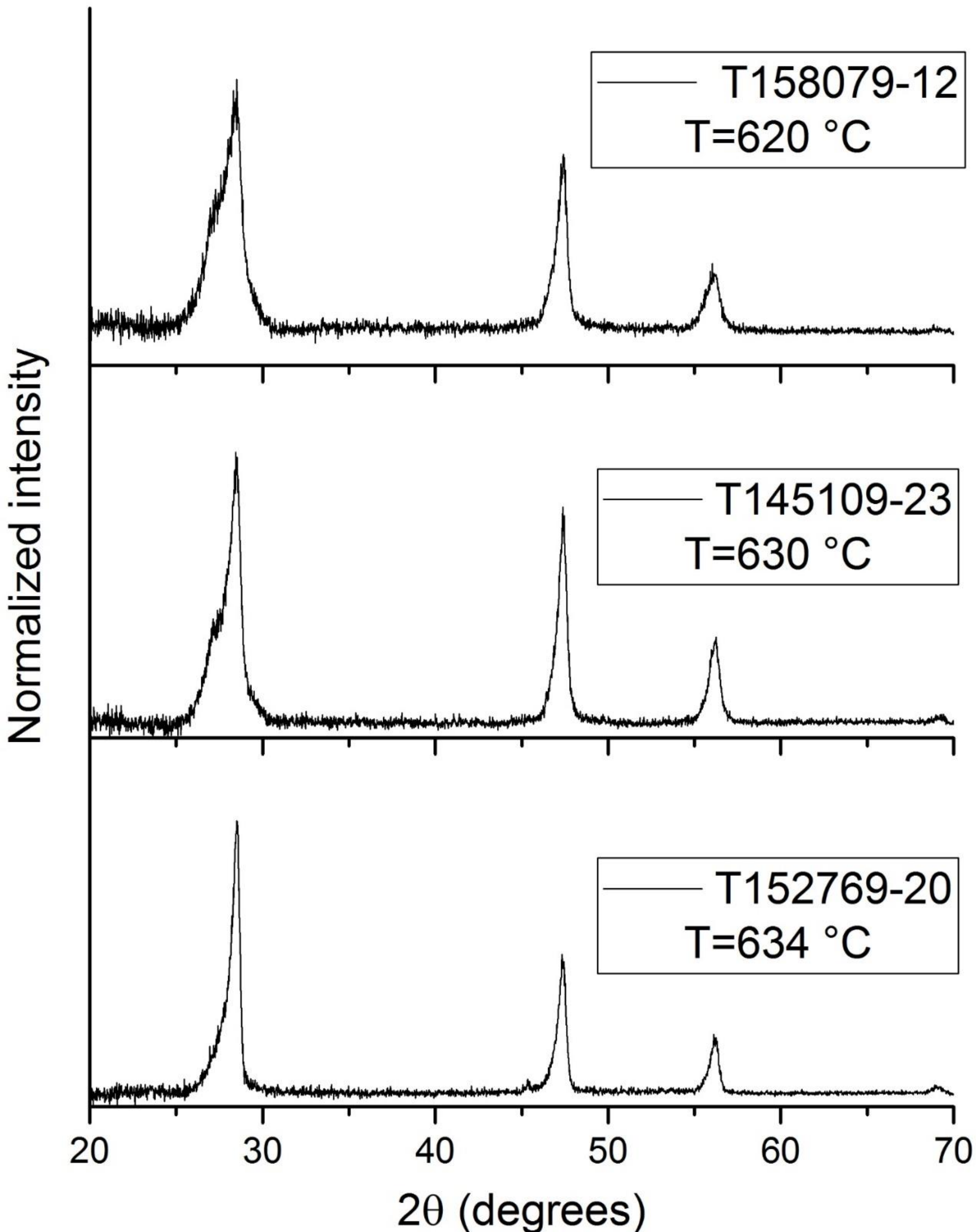
XRD results

In the figure are shown the XRD measurements of the samples



- *The presence of 4 main peaks:*

  28.5° (111)

  47.4°(220)

  56.0° (311)

  69.4° (400)

are due to the fcc structure of Silicon (JCPDS card: 00-027-1402).

- *The line shape of the peak at 28.5° is the convolution of the Si and SiO2 (about 26.9°)signals (JCPDS card: 01-078-1256).*

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XRD summary table

- The grain size of the polysilicon films was estimated by using the Sherrer formula using the peak at 47.4

Sample	poly dep Temperature	Poly Grain size estimated by XRD (nm)
T158079-12	620	13.1
T145109-23	630	14.6
T152769-20	634	16

- As PolySi Temperature deposition increase , poly grain size increase

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TEM Analysis

- *TEM Image collected for x-section and planar sample.*
- *Poly grain measurement: collected 10 different images on the same sample. Measure of about 10 grains per image, in x-y direction.*
- *The grain size was calculated as the medium value of x-y dimensions.*

Instrument :TEM FEI TECNAI G2 F30 S TWIN

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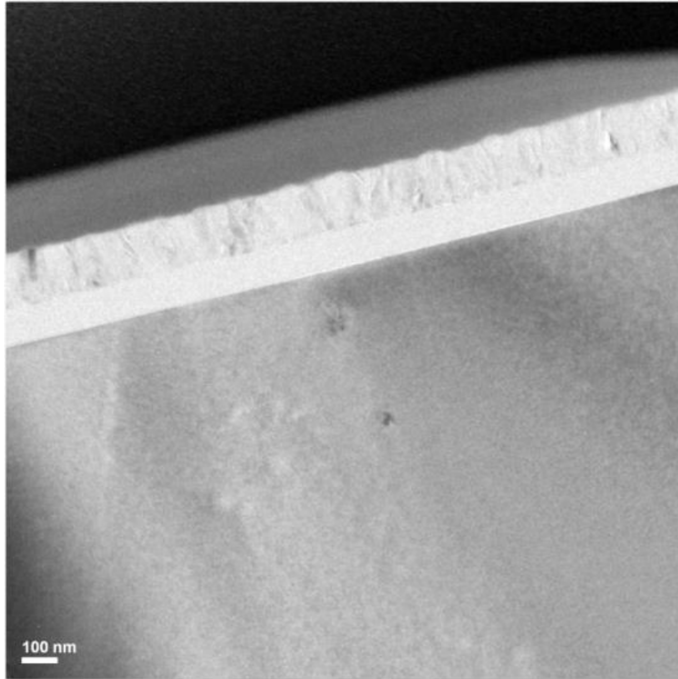
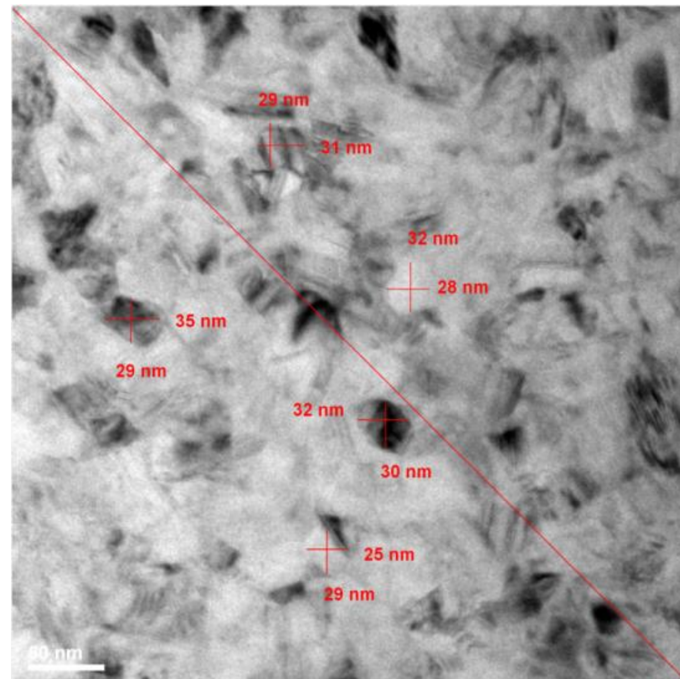
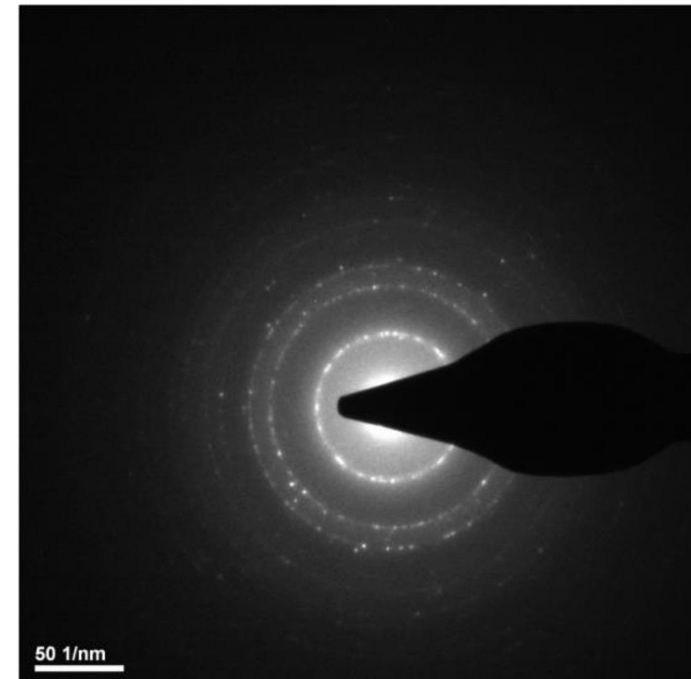
Lot ID T158079 - Wf#12 **Poly Temp 620 furn Posit TOP**







poly dep Temperature	Poly Thickness (Ang)	# grain boundaries	Grain Size (nm)
620	1550	24	35.4

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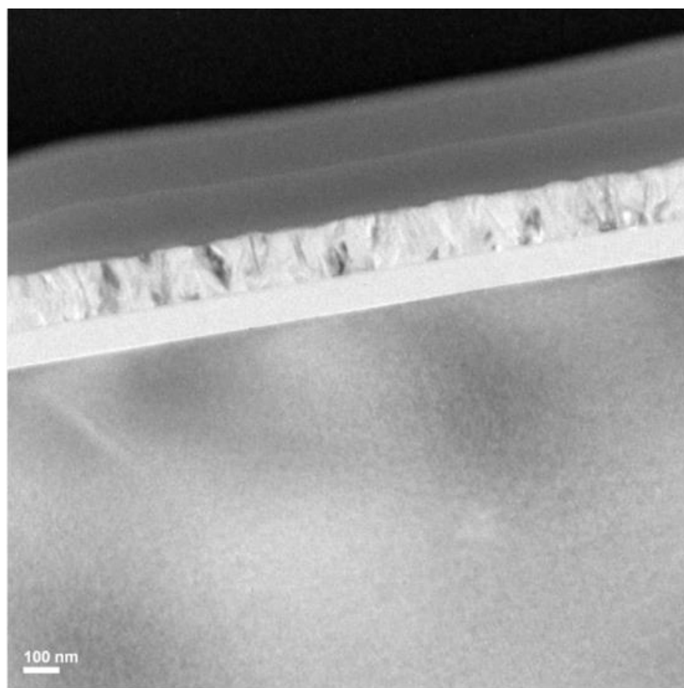
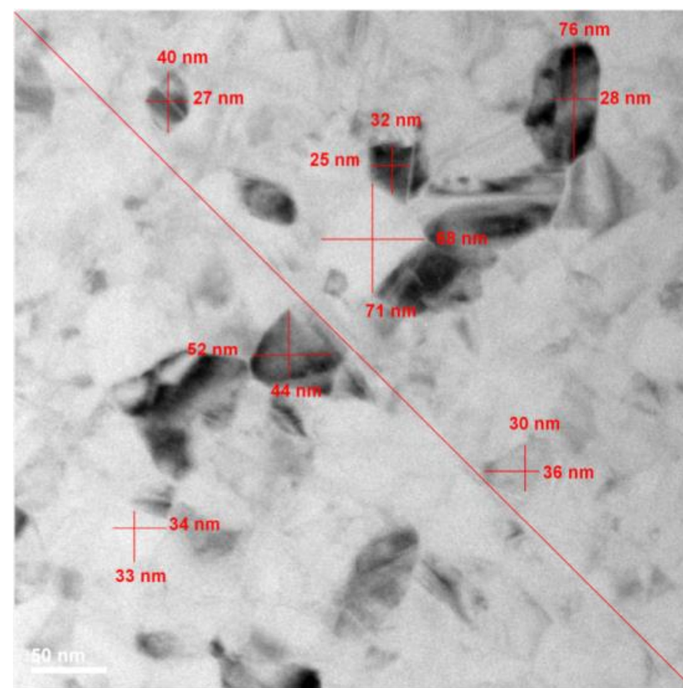
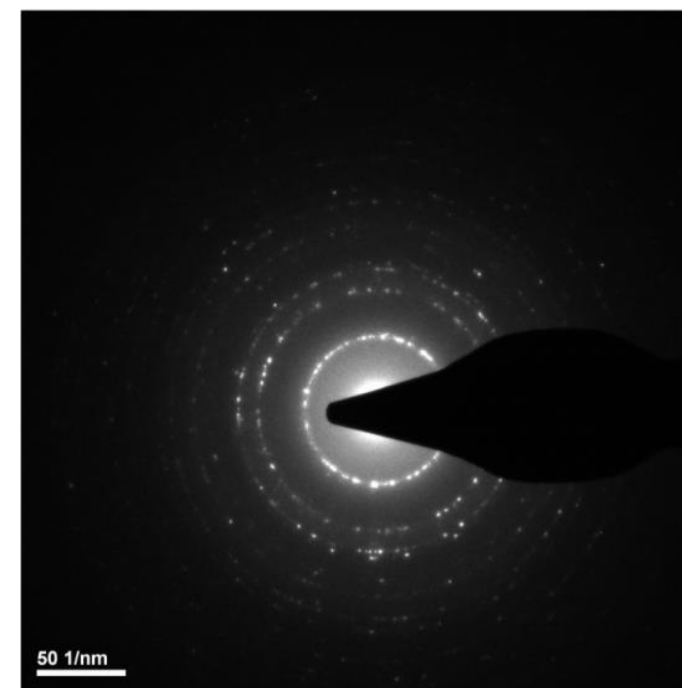
Lot ID T145109 - Wf#23 **Poly Temp 630 furn Posit TOP**







poly dep Temperature	Poly Thickness (Ang)	# grain boundaries	Grain Size (nm)
630	1540	24	43.4

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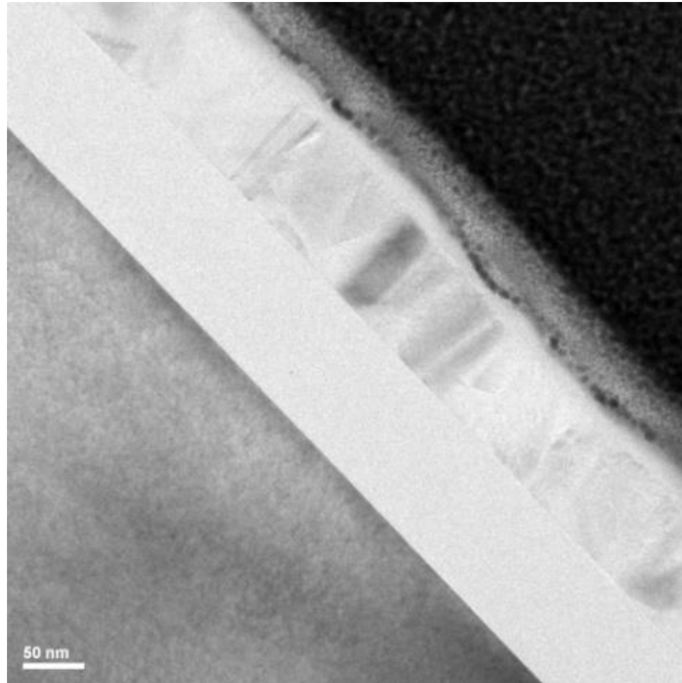
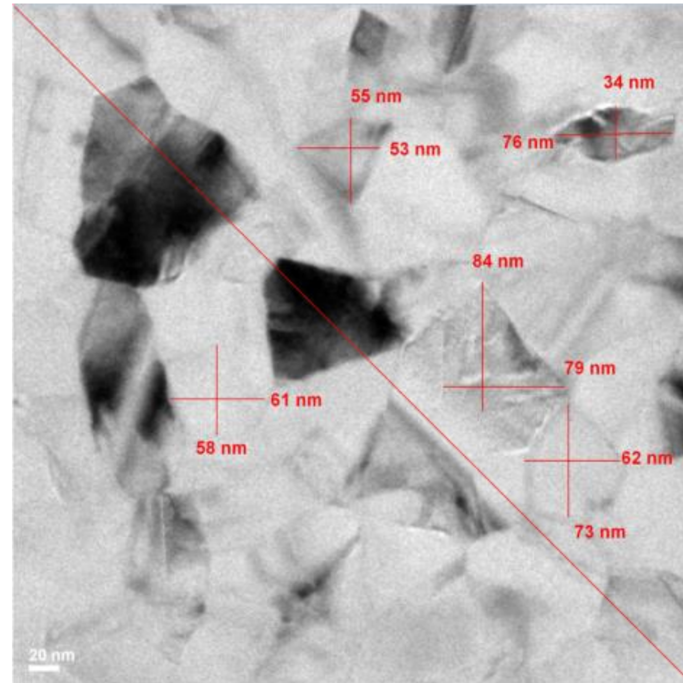
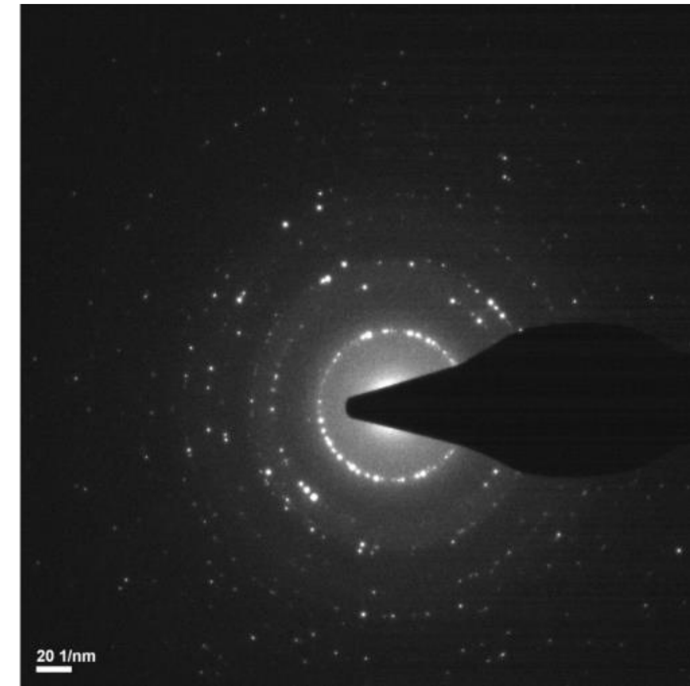
Lot ID T152769 - Wf#20 **Poly Temp 634 furn Posit TOP**







poly dep Temperature	Poly Thickness (Ang)	# grain boundaries	Grain Size (nm)
634	1030	16.9	59.5

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TEM Result summary table

	TEM		
poly dep Temperature	Poly Thickness (Ang)	# grain boundaries	Grain Size (nm)
620	1550	24	35.4
630	1540	24	43.4
634	1030	16.9	59.5

- *As PolySi Temperature deposition increase ,poly grain size increase*

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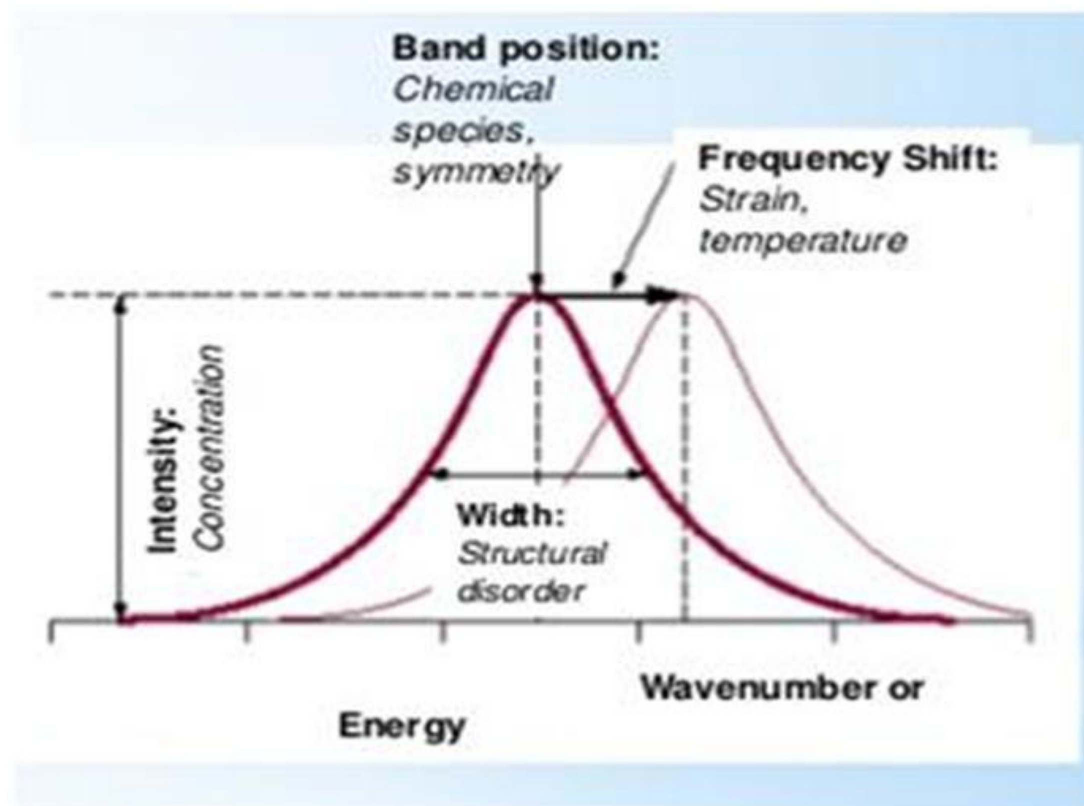
Raman Analysis

- ***Raman scattering has been used extensively to characterize semiconductor properties because materials such as Si, SiGe, InGaAs, GaAs, GaN, and graphene exhibit precise, distinct Raman bands.***
- ***Raman spectroscopy is also effective in evaluating the crystallinity of polysilicon***



Instrument : Raman InVia Renishaw .Laser :Nd:YAG - 532 nm (green)

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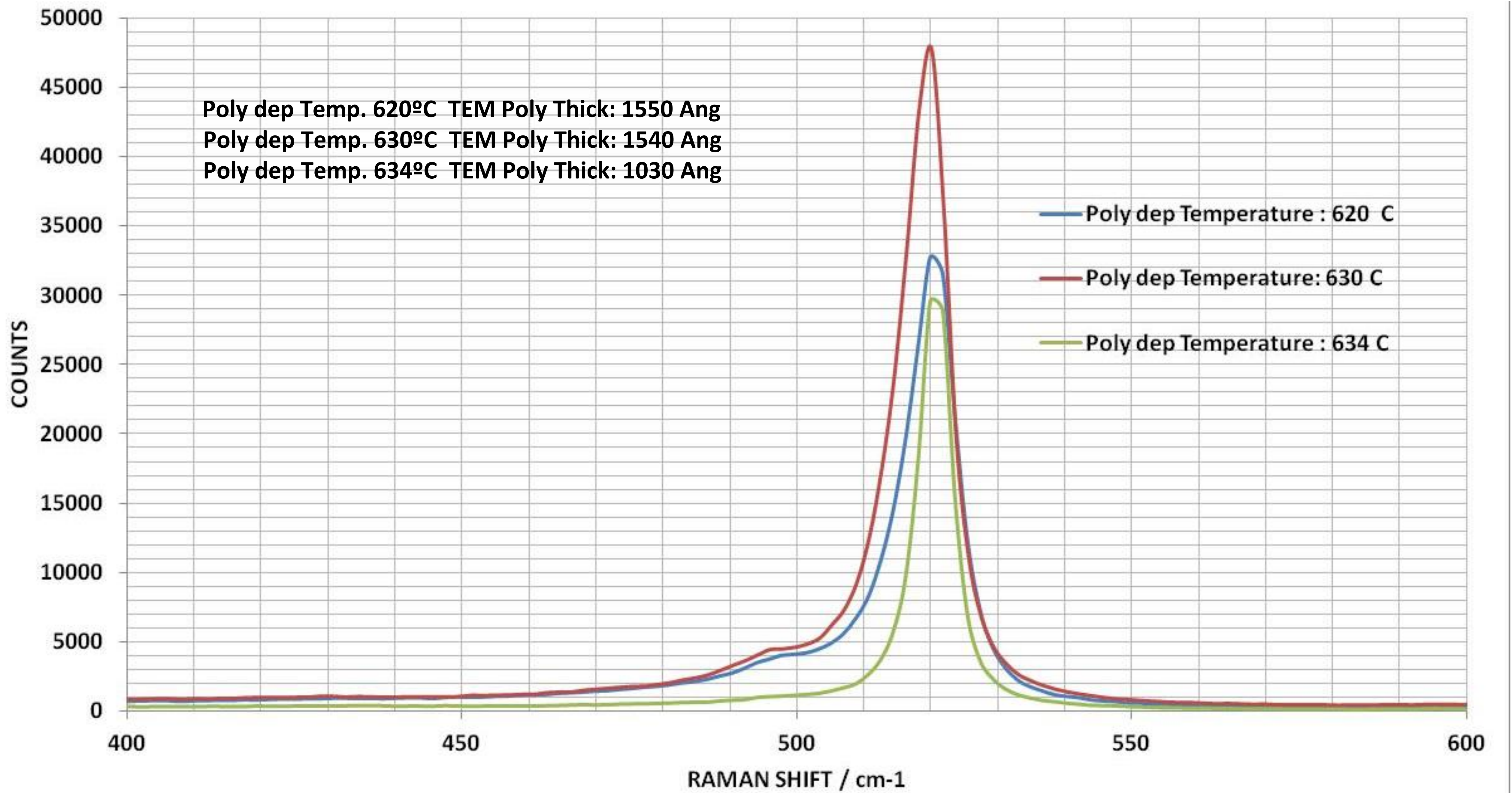
Raman Spectrum Vs Poly deposition Temperature Sample

Raman Shift range: 400-600 (cm-1)



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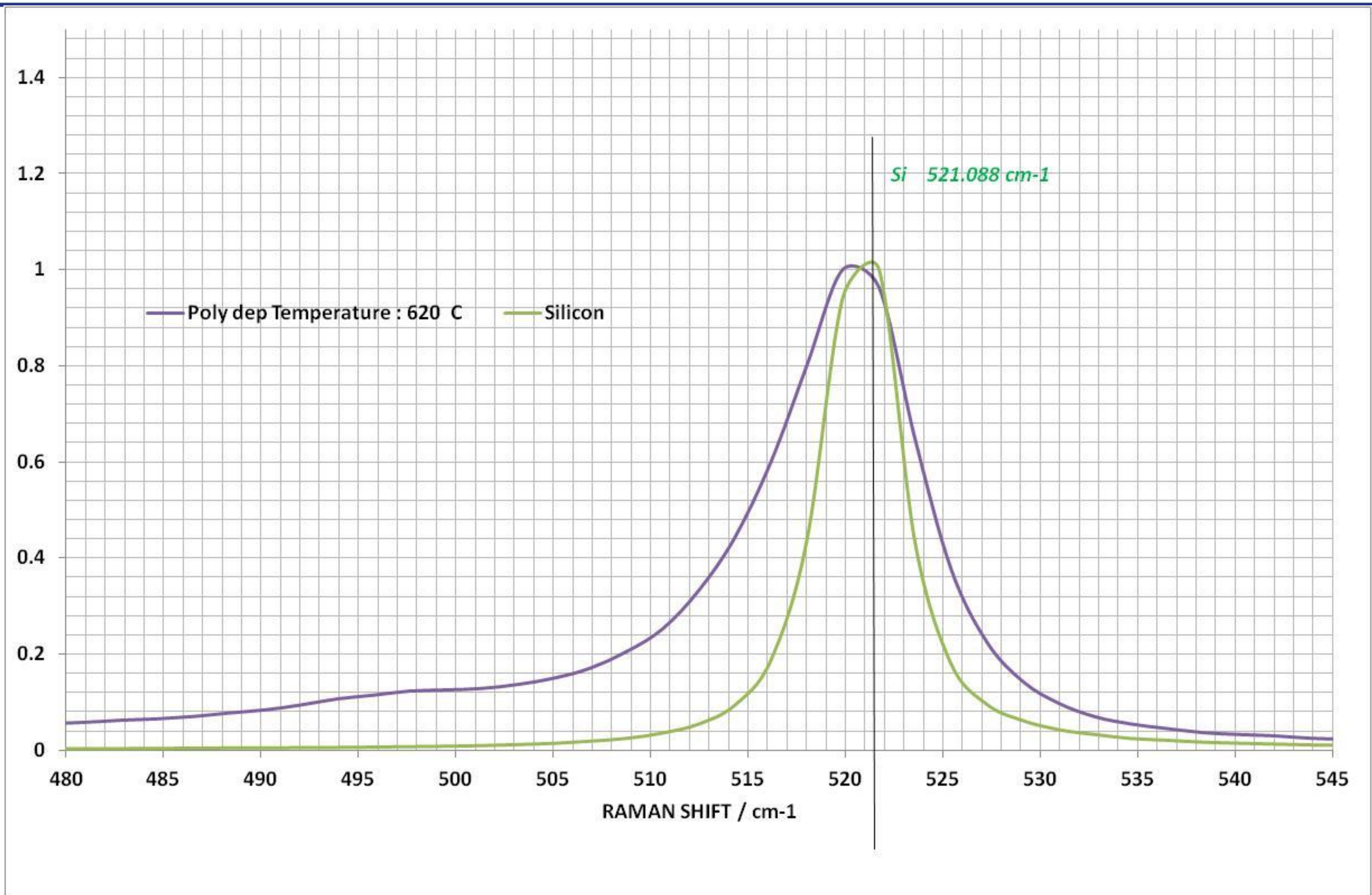
Normalized Raman Spectrum :
Poly deposition Temperature 620 C



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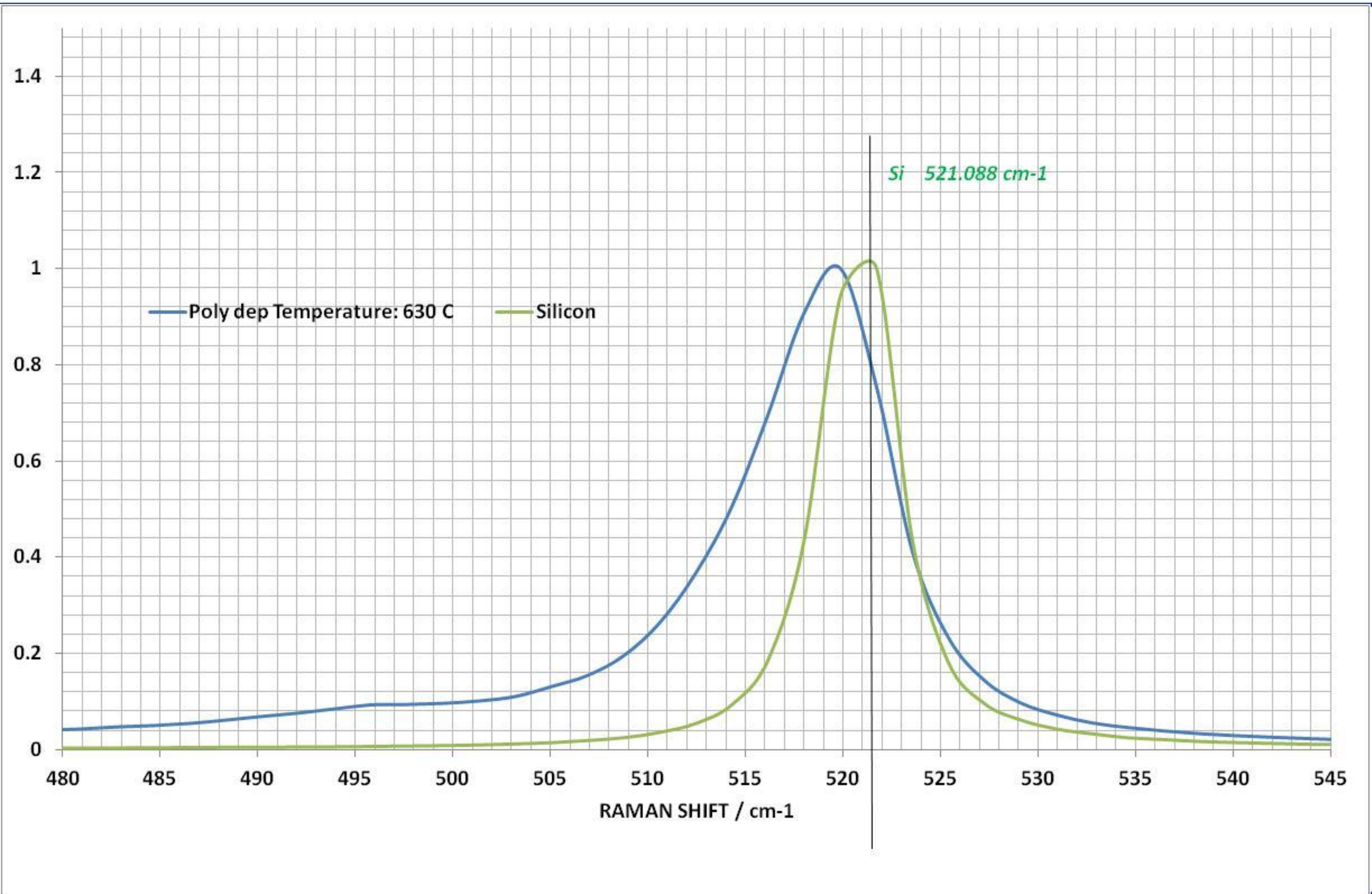
Normalized Raman Spectrum :
Poly deposition Temperature 630 C



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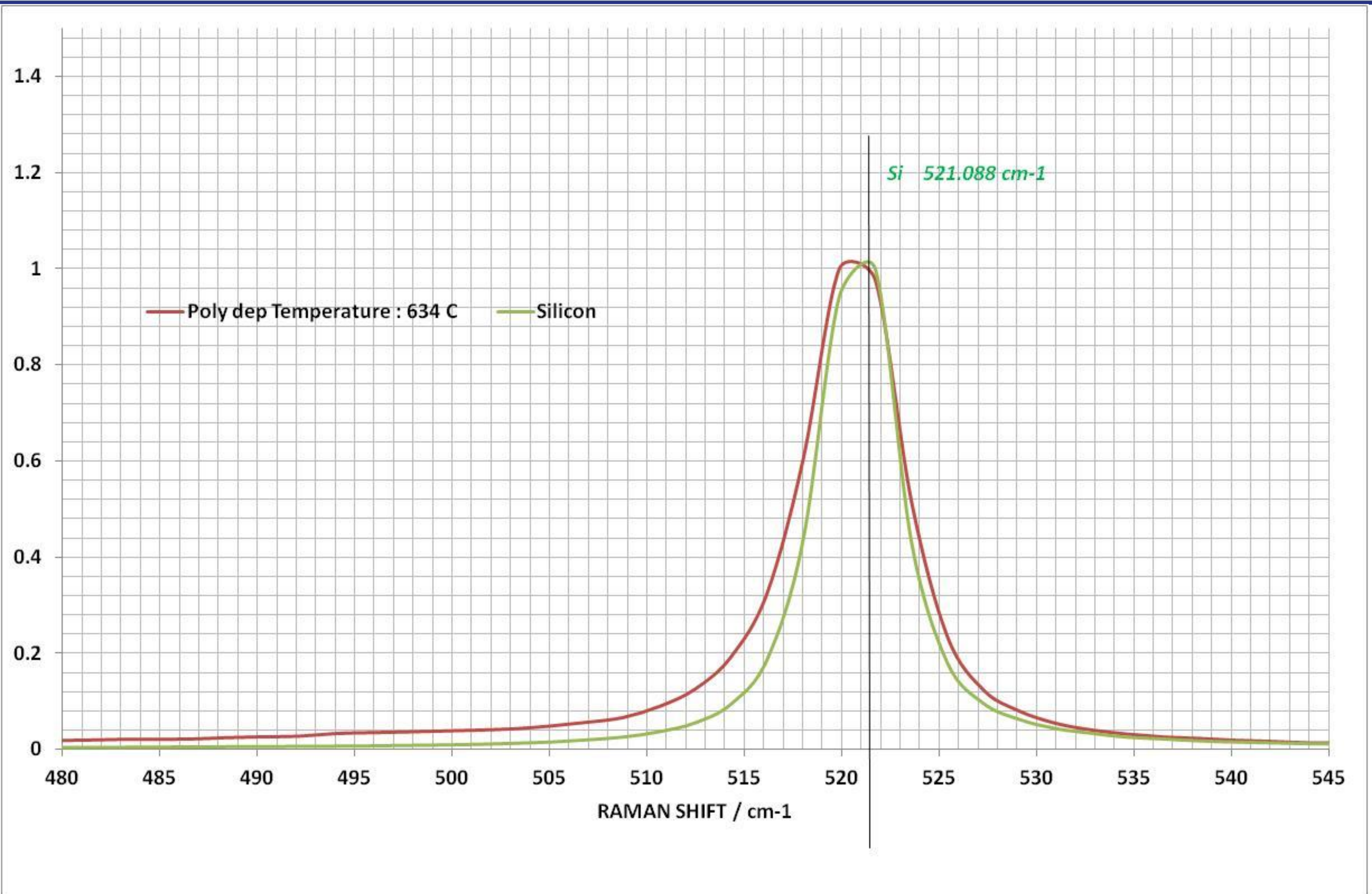
Normalized Raman Spectrum :
Poly deposition Temperature 634 C



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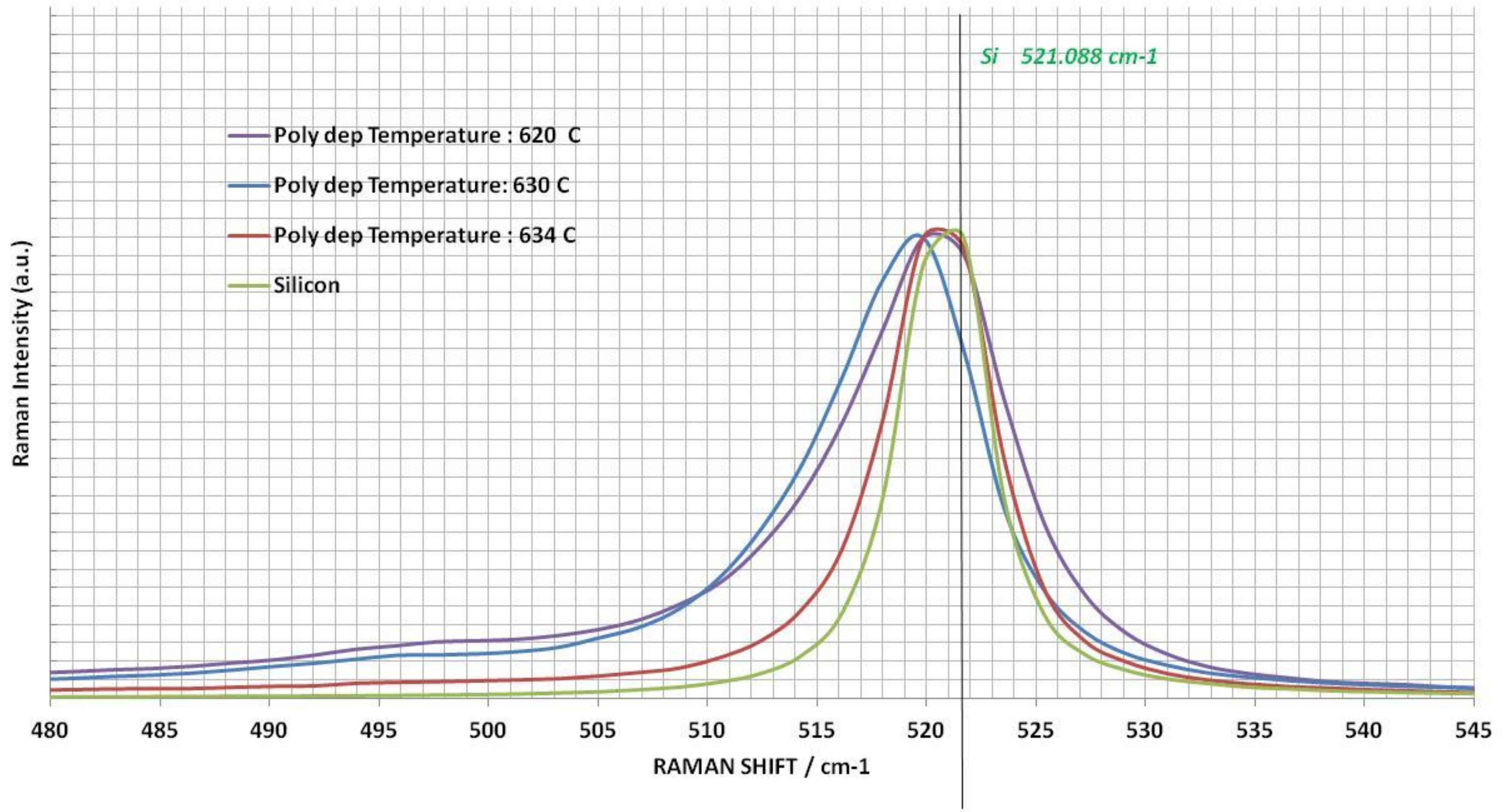
Normalized Raman Spectrum Vs Poly deposition Temperature



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Raman Result summary table

poly dep Temperature	Center Peaks position (cm-1)	Width
620	519.89	9.318
630	519.02	8.711
634	520.58	5.727

•*The reduction of the peak width FWHM (Full Width at Half Maximum) indicates that a more perfect crystalline lattice is obtained*

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XRD-TEM-RAMAN Result summary

	XRD	TEM			RAMAN	
poly dep Temperature	Poly Grain size estimated by XRD (nm)	Thickness (Ang)	# grain boundaries	Grain Size (nm)	Raman Peaks position (cm-1)	FWHM of Raman Cristalline Peak (cm-1)
620	13.1	1550	24	35.4	519.89	9.3
630	14.6	1540	24	43.4	519.02	8.71
634	16	1030	16.9	59.5	520.5	5.7

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CONCLUSION

- ***As PolySi Temperature deposition increase ,poly grain size measured by XRD and TEM increase as well and the half width of the Raman Peak reduces that means that a crystalline lattice structure is obtained***

This work showed a good correlation among XRD /TEM and Raman poly silicon characterization. Raman emerges as the most useful non destructive technique to characterize and monitor in line transistor poly-Si gate processes

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